12.6 A 14b 100MS/s Digitally Self-Calibrated Pipelined ADC in 0.13µm CMOS

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Highly integrated communication or imaging systems require a high-speed high-resolution ADC core with low supply voltage and low-power consumption. In conventional pipelined ADCs, the front-end S/H and the first MDAC require the highest accuracy and consume the most power. In this paper, an architecture that does not need a dedicated front-end S/H and thus saves power is described. A charge-compensation circuitry is used to avoid ISI.

A viable solution to implement resolutions of 14b and beyond is digital background calibration [1, 2]. This ADC utilizes the advantages of digital calibration to achieve a 14b resolution. The gain and matching errors of the analog circuitry are fully compensated by the proposed digital calibration scheme, which allows the usage of a low-gain opamp. The 14b pipelined ADC is implemented in a 0.13µm digital CMOS process with a power consumption of 224mW. The proposed architecture is designed for a low supply voltage of 1.5V and prepares the way to nanometer technologies with supply voltages smaller than this.

The ADC, shown in Fig. 12.6.1, consists of four stages and a final 4b ADC. The first two stages contain an MDAC with an amplification of 8. The following two stages are implemented with an interstage gain of 4 [3]. In addition to the standard pipeline architecture a digital calibration block is necessary that has to be driven by a pseudo-random signal generator. The ADC is designed by means of a fully differential switched-capacitor implementation. Due to the low voltage, simple analog parts such as Miller opamps (Fig. 12.6.1) are used for critical circuit parts. The standard Miller architecture does not need any stacked device and operates reliably down to a very low supply voltage. There are only two transistors in the output stage which ensure a high output swing. The disadvantage of the simple Miller opamp is the limited open loop gain (A_0), which will introduce a major gain error. In this ADC, the opamp has an A_0 of 44dB and a GBW of 2GHz. The opamp in the first stage draws a current of ~100mA which is already 68% of the whole current of the ADC. The limitation of A_0 is solved by digital calibration of the first two stages. The rest of the pipe is a standard multi-bit pipelined architecture. All blocks are designed in a standard digital 0.13µm CMOS process without any high-voltage device.

The block diagram of the proposed digital background calibration is shown in Fig. 12.6.2. This calibration method is applied identically to the first two stages. For simplicity, only one stage is described in the following section. A pseudo-random sequence (PRS) is generated digitally and fed by a digital-to-analog subconverter (DASC2) at the summing node of stage 1 (A1) to the signal path. The following stages are included in ADSC2. The PRS sequence is multiplied in the digital domain by an estimated gain (gain_d) and subtracted from the digital word generated by ADSC2. The remaining signal is correlated with the PRS sequence and the correlation output (err) is used to tune the estimated digital gain. If the estimated gain (gain_d) matches to the interstage gain (gain_a) the signal err is reduced to zero. This principle allows the calculation of the interstage gain of the amplifier.

It is obvious that the additional DASC2 can now be merged with DASC1, which is the normal operating DASC of stage 1. This merge leads to an extension of DASC1 by an additional calibration capacitor shown in Fig. 12.6.3. The calibration C and the connected switches form the DASC2 of Fig. 12.6.2. The rest of the switched-capacitor circuitry is a standard multi-bit architecture. This configuration of Fig. 12.6.3 allows the calculation of the DAC weight of the calibration capacitor according to Fig. 12.6.2. To calculate the DAC weight of the other capacitors C1 to Cn the capacitors must be exchanged with the calibration capacitor. This is realized using a multiplexer. The difference in the calculated gain_d values of every capacitor reflects the DAC error.

The missing dedicated S/H introduces several problems. One major disadvantage is the visibility of a quantized charge at the sampling capacitor. The sampling capacitor is charged to a quantized voltage (b/k×Vref) depending on the decision of the flash ADC which is based on the previous sample (Fig. 12.6.4). Thereby, b is an integer number with the maximum value of k, and k is the number of comparators used in the flash ADC. This charge is visible to the input during the next sampling period and will cause an ISI because b is correlated to the previous sample. To avoid this negative effect a dummy sampling capacitor is used and is charged during the amplification phase to the negative quantized voltage which is quite simple in a fully differential circuitry. This negative charge is connected to the input during the next sampling period and cancels completely the charge of the real sampling capacitor. This additional dummy capacitor increases the SNR and THD of the ADC by up to 20dB.

The proposed ADC is implemented in a 0.13µm 1P 6M CMOS process. MIM capacitors are used. The ADC core occupies an active area of 1.02mm^2 and dissipates 224mW at 100MS/s which results in 1.12pJ/conversion-step. Figure 12.6.5 shows the die micrograph of the prototype ADC. The S/H of the ADC is matched to the S/H of the first stage. The input of the ADC is directly connected to the pads. The measured INL and DNL in a non-calibrated mode and in a calibrated mode are shown in Fig. 12.6.6. The digital calibration improves the INL of the ADC from 43 to 2LSB. Due to a design weakness in the backend ADC all measurements are done with a supply voltage of 1.7V. The increased power is considered in all figures. The SNR plot and the THD plot for the calibrated ADC are shown in Fig. 12.6.6. For all plots the dummy sampling capacitor is used to improve the performance. Only one reference curve shows the degradation of the SNR and THD without the use of the dummy capacitor with a 5MHz input signal. The reference voltage is provided externally to a reference voltage buffer which is implemented on the chip. The state machine and the pseudo random generator are also integrated on the test chip. The calibration algorithm is not implemented on chip but is applied in a post processing routine to the ADC output data. The measured performance of the prototype ADC is summarized in Fig. 12.6.7.

References:

[1] I. Galton, "Digital Cancellation of D/A Converter Noise in Pipelined A/D Converters" *IEEE Trans. Circ. Syst. II*, vol. 47, no. 3, pp. 185-196, Mar., 2000.

[2] H. Liu et al., "A 15b 20MS/s CMOS Pipelined ADC with Digital Background Calibration," *ISSCC Dig. Tech. Papers*, pp. 454-455, Feb., 2004.

[3] P. Bogner "A 28mW 10b 80MS/s Pipelined ADC in 0.13µm CMOS" *IEEE Int. Symp. Circuits and Sytems*, vol. 1, pp. 17-20, May, 2004.

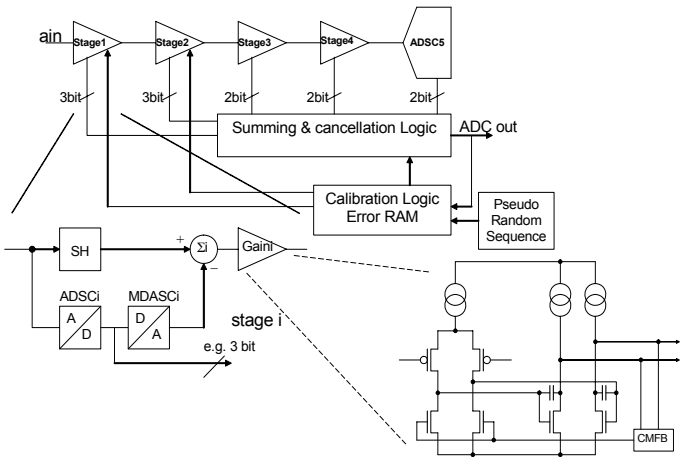

Figure 12.6.1: ADC architecture.

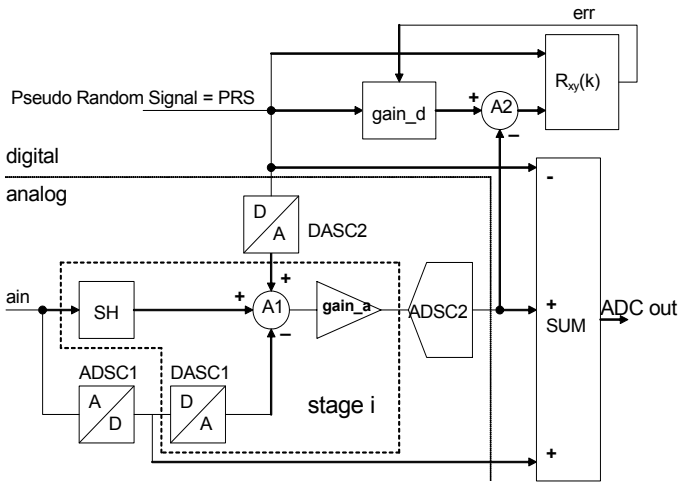

Figure 12.6.2: Calibration concept.

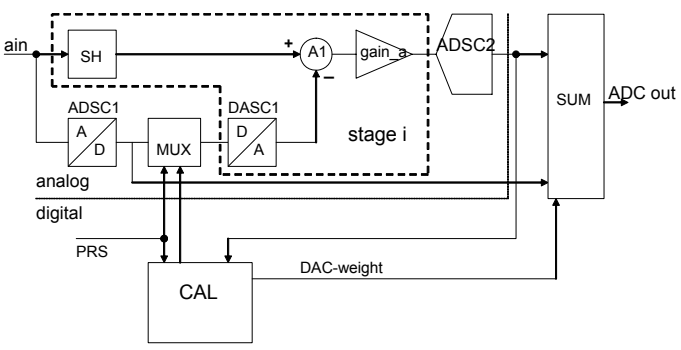

Figure 12.6.3: Extended MDAC and MUX of stage 1&2.

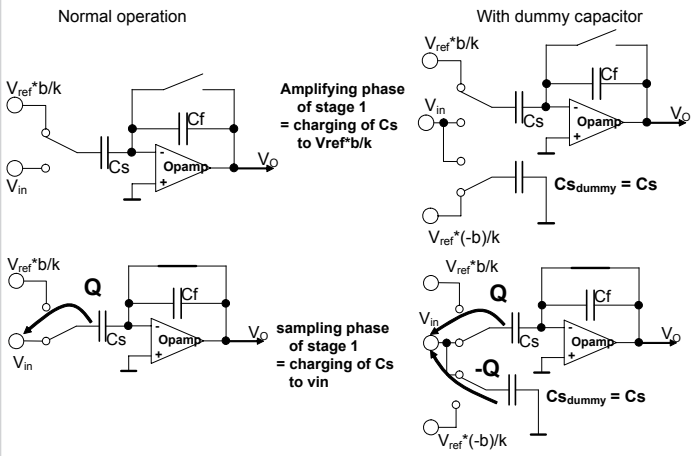

Figure 12.6.4: Dummy capacitor for charge cancellation.

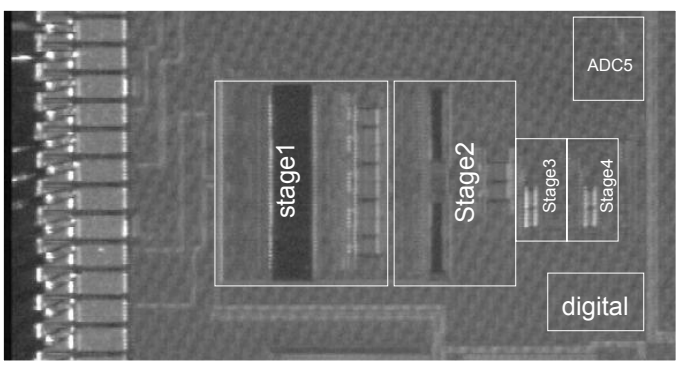

Figure 12.6.5: ADC die micrograph.

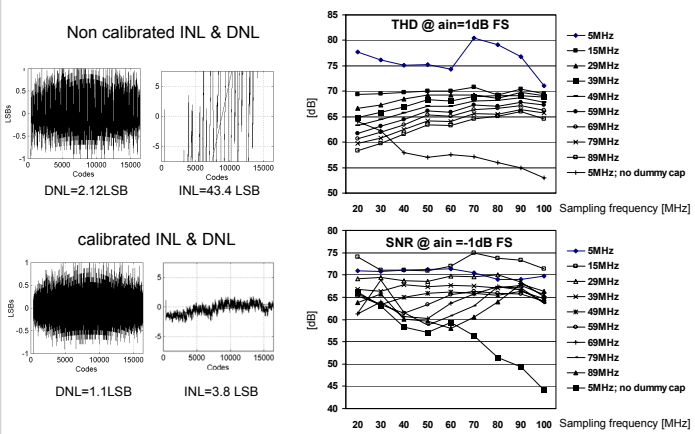

Figure 12.6.6: INL, DNL, THD, and SNR versus sampling frequency.

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Technology	Standard 0.13µm CMOS, 6 Cu-metals
Resolution	14 bit
Conversion Rate	100MSamples/s
Supply Voltage	1.5V
Input Range	$1.5V_{pp}$, differential
Power Consumption	224mW
SNR	71.4dB @ f_{in}=15MHz @ -1dBFS 66.5dB @ f_{in}=39MHz @ -1dBFS
THD	79.1dB @ f_{in}=5MHz @ -1dBFS 69dB @ f_{in}=39MHz @ -1dBFS
INL	±2 LSB
DNL	±1.1 LSB
Active ADC core area	$1.02mm^2$

Figure 12.6.7: Performance summary.

